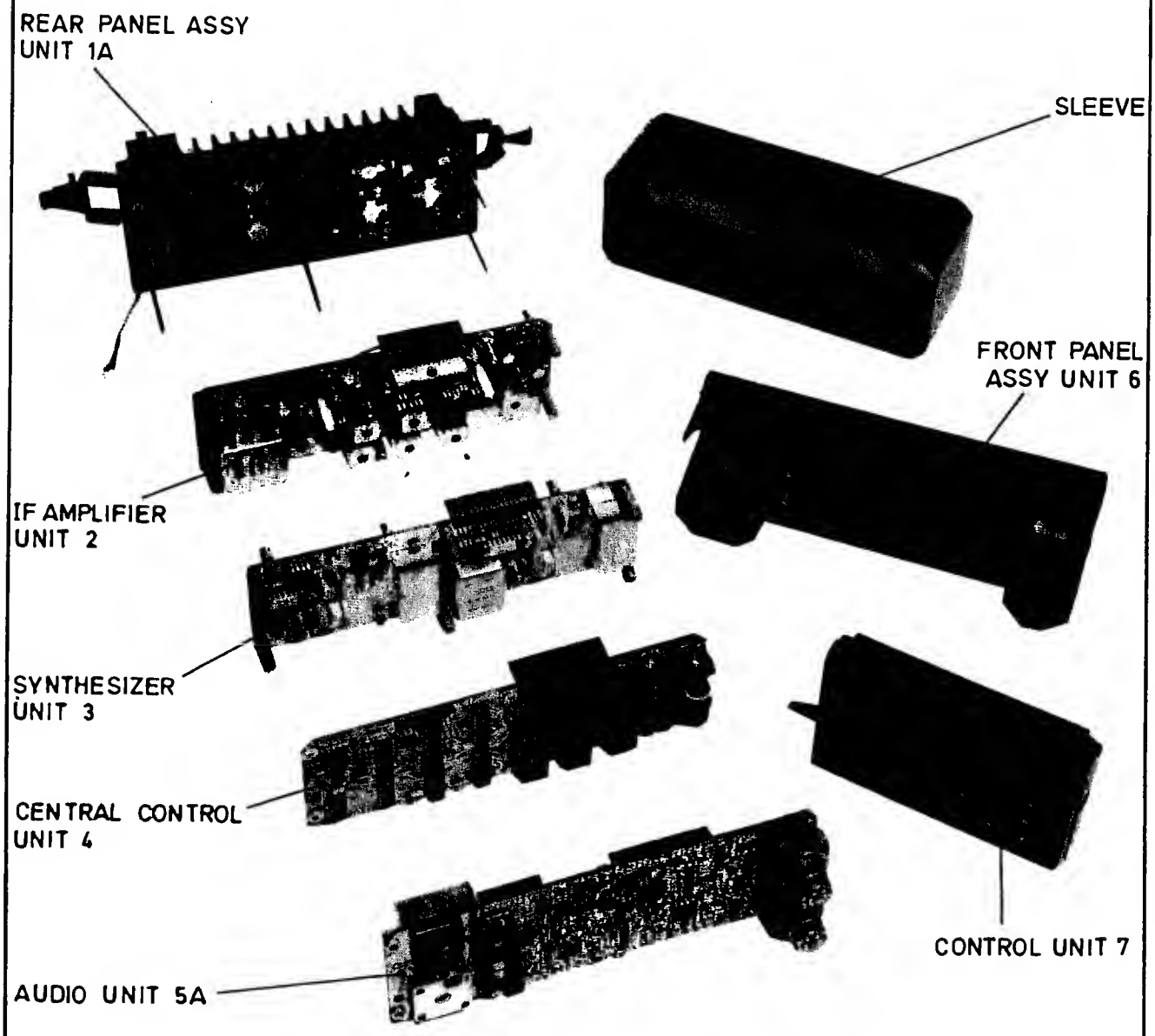


RACAL

TH9346
BCC 39A

Internal View

Fig.19

CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1 The BCC 39A is a high power HF manpack radio oriented towards long range patrol operation using short burst transmissions (CW or data using FSK keying from an ancillary unit). The unwanted radiation from the receiver is kept at a very low level and when using the associated ATU, the BCC 565, the tuning times are very short. Operation can take place using single frequency simplex and two frequency simplex (half duplex). The controls (except on/off and selection of 1F, 2F) are on a removable unit which may be extended, using a special cable, for use by an operator on the move. The radio, the control panel and the connector are separately sealed. The BCC 39A operates in Upper Sideband and Lower Sideband modes and uses American style connectors.

FACILITIES

2 The BCC 39A provides a high power (50 W) Transceiver (TCVR) in a very small size. Operation with its associated ATU, the BCC 565, (Power out reduced to 25 W) can be carried out with the ATU fixed to the TCVR or separated from it by up to 50 m of coaxial cable. No other cable is required as supply and signalling to and from the ATU are carried by the coaxial cable as well as the RF signal.

3 The controls for the TCVR are carried on a removable unit (except for the on/off switch and selection of 1F, 2F) which allows the radio to be used with the controls available to the operator on a short cable with the radio mounted on the operator's back.

4 Both the TCVR and the ATU have memory to store up to 10 channels, with frequency data for the TCVR and relay setting data for the ATU. This allows channel changing without the need to radiate. When an active tune sequence is required it is initiated by a change of channel frequency or by pressing a TUNE key. The tune sequence is very short, typically less than 300 ms.

5 Operation in normal single frequency simplex is provided and, by setting the on/off switch to 2F, two frequency simplex. Then transmission and reception take place on two different channels, and so, frequencies. Channels 0 - 4 are allocated to Transmitting and 5 - 9 to Receiving.

6 A search mode permits the operator to change frequency by increments of 100 Hz at a slow or fast rate to look for a clear channel or to interoperate with older, less stable radios.

7 Full information of operating mode and frequency is given by an illuminated Liquid Crystal display which also gives an indication of received signal strength, transmitted power and battery voltage. The Test mode also provides further built in test facilities defined in Chapter 3.

CONTROLS

8 On/Off switch

Z	Zeroise radio memory
OFF	All power off (radio memory retained)
AUX	Radio power off, power to auxiliaries on.
ON 1F	Normal operation, single frequency simplex
ON 2F	Normal operation, two frequency simplex.

A mechanical stop is placed between Z and OFF, released by pressing a button at the side, to avoid zeroising the memory unintentionally.

NOTE:
Zeroise can only take place if a battery is connected.

9 Keyboard (on removable panel)

Digits 0-9 are used to:

Set frequency
Set channel number

Arrow keys are used to:

▲ Increase volume in 8 steps

▼ Decrease volume in 8 steps

NOTE:
They are also used to increase or decrease frequency when in "search" mode.

On switch on volume is set to a mid value.

MODE Using toggle action selects in sequence

USB/Voice, display USB -
LSB/Voice, display LSB -
USB/CW, display USB CW
LSB/CW, display LSB CW

PWR Using toggle action selects in sequence:
High power (50 W) display - HP
Low power (5 W) display - LP

TUNE — Initiates an active tune on selected frequency.

NOTE:
Changing to a new frequency (or channel if untuned) automatically initiates an active tune when PTT is next operated. In two frequency simplex the TUNE key initiates an active tune on the "receive" frequency, the "transmit" frequency is automatically tuned when the PTT is next operated.

SET — Sets (stores) the following digits into memory as frequency.

CH — Single frequency simplex:
Sets the working channel when followed by a digit (0 to 9).

Two frequency simplex:
Changes the display to show the Rx or Tx channels and frequency when toggled. When followed by a digit it sets the working channel (Tx 0-4, Rx 5-9).

T — Test key. An active test sequence is initiated when the Test key is operated. Also used to illuminate the display.

DISPLAY

10 The display is divided into 16 areas as follows:

1	USB	
2	LSB	
3	◇	Indicates search mode
4	CW	Note: Voice/data mode has no display
5	HP)	Power selection
6	LP)	
7	Rx)	Used when in two frequency simplex mode to show whether
8	Tx)	the channel and frequency displayed is for Tx or Rx. Both Tx and Rx are displayed in the single frequency simplex mode. NOTE: Tx or Rx does not indicate that the radio is transmitting or receiving.
9	0-9	Channel number
10	Bars	5 Horizontal bars. Shows 0 to 5 bars to indicate the received signal level (the more bars the stronger the signal). When transmitting the bars display the power output relative to that selected. During a Test sequence the bars show the battery voltage.
11-16		Frequency of the selected channel (with a fixed decimal point after the first two digits) in MHz.

CONNECTORS

11

Coaxial socket 50 ohm	Antenna connector (50 ohm) BNC (connects to ATU or dipole antenna cut to length)
Audio socket (x2) AUDIO	Audio socket 5 way US type to MIL-C-55116 A Earth return B Phones C PTT D Microphone E +24 V for auxiliaries
Control panel connector	Three way special A Earth B Supply, +5 V C Data, 5 V logic
Supply terminal (x2) (rear panel)	Battery connector special +24 V 0 V

BATTERY

12 24 V 4Ah NiCd rechargeable to "Clansman" interface
or
24 V 16Ah $LiSO_2$ primary to "Clansman" interface.

FUSES

13 A special wired in fuse link is fitted to the rear panel of the BCC 39A.

CONSTRUCTION

14 The BCC 39A is of modular construction and uses printed circuit and large scale integration (l.s.i.) techniques throughout. The radio is mounted in an aluminium alloy, sealed box-frame comprising:

(1) The Front Panel Assembly

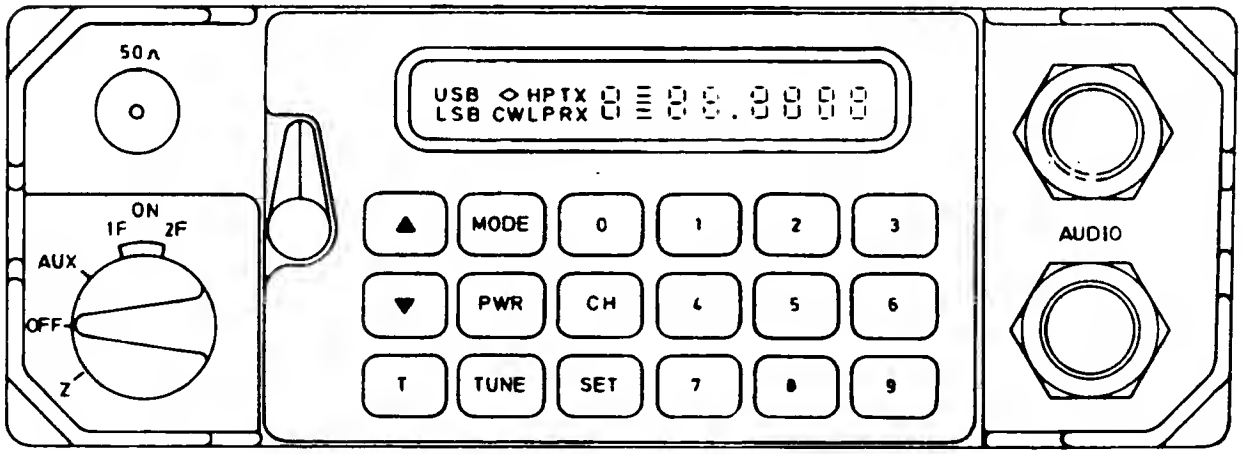
(2) The Rear Panel Assembly on which is mounted 5 plug-in discrete, units.

(3) The Sleeve Assembly, to which the Front Panel Assembly and the Rear Panel Assembly secure and which protects the interior of the radio.

15 The radio is sealed by toroidal seals fitted in the mating surfaces between the Front and Rear Panel Assemblies and the Sleeve. The keyboard switches and the LCD display are contained in a separately sealed unit, which can be removed from the Front Panel for remote operation. A sealing test point is provided at the Rear Panel Assembly and on the Keyboard.

16 With the exception of the PTT switch and on/off 1F, 2F switch, all the operator controls are mounted on the Keyboard and Display Unit. The design and arrangement of these controls is such as to provide ease of operation under all conditions of service.

17 The overall dimensions and weight of the radio are as detailed in the Technical Specification.



Front Panel Layout Fig.1.1

CHAPTER 2

CIRCUIT DESCRIPTION

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APPENDIX

APPENDIX 1 BCC 39A KBS FORMATS AND PROTOCOL

CHAPTER 2

CIRCUIT DESCRIPTION

SIGNAL SUMMARY (Fig 18)

1 The signals annotated in this equipment normally use a three letter code. The signals are:

AFR	AF Receive
AFT	AF Transmit
AF1	AF Volume Control 1
AF2	AF Volume Control 2
AF3	AF Volume Control 3
BATT	Battery supply
BSW	Battery switched
CPL	Control Power Select Low
CPS	Control Pressel
DCE	DC Earth
GCF	Gain Control Function (AGC line)
KBS	Key Board Signal
KCW	Keyed CW (oscillator)
KFR	Not Used
KVO	Not Used
LO1	Local Oscillator 1
LO2	Local Oscillator 2
LO3	Local Oscillator 3
MSA	Mode Switch Audio
PMF	Power Measure Forward
PMR	Power Measure Reverse
RSI	Receive Signal Input
SD1	Synthesizer Data 1
SD2	Synthesizer Data 2
SWA	Switch A (System switch)
SWB	Switch B (System switch)
SYC	Synthesizer Clock
SYF	Synthesizer Frame
SYL	Synthesizer Lock
TSD	Transmit Signal Drive
TNE	Tone Enable (Error Tone)
TUS	Tuning Unit Supply
5VC	5 V constant
12VC	12 V constant
12VRX	12 V Rx mode
12VTX	12 V Tx mode
20VC	20 V constant

POWER AMPLIFIER (UNIT 1A) See Fig 1.

2 Unit 1A contains the transmitter power amplifier systems and the TX/RX relay RLA. In Receive, the incoming signals are passed from the low pass (30 MHz) filter on the AF unit (5A) via RLA to the receiver signal input (RSI) port on unit 2.

3 In Transmit the SSB signal (from unit 2) at TSD is amplified, and the signal passed via the VSWR and power sensor to the low pass filter on Unit 5A. The VSWR and power information is transported as analog signals to the central control for measurement. The central control then uses the measured values of the PMF and PMR signals to compute the AGC setting required for optimum operation.

4 The 24 V battery supply is applied to PL1 and PL2. The input is protected against excessive current by FS1 and reverse polarity connection by D1. The 24 V supply is stabilised to 18 V by the action of circuit TR6, TR7, D1, D3 and associated components.

5 The supply allows TRs 2, 3 and 4 to switch on the bias for the power amplifier circuit of TR5 and associated components. It sets the operating point of TR5 by sensing the drain current with R10 (5.1 ohm) and controlling the gate voltage with TR3. The reference point for the circuit is set by R4/R5.

6 TR9, 12, 14 and 15 sets the operating point for TR10, 11, the power amplifier driver stage. R20 senses the drain current and TR12 controls the gate voltage. The action of R31, 32, 33 and TR15 sets the reference. TR15 changes the reference between high power and low power modes.

7 TR20, 23, 21 and 22 control the current for the sliding bias for the high power amplifier stage TR18, 19. R46, R50, R53, R57 and TR21 sense the source current of TR18. R49, R51, R54, R58 and TR22 sense the source current of TR19. TR23 and TR20 generate the gate voltage for TR18, 19 and R60 sets the static bias.

8 TR16 is the high/low power switch which is controlled by CPL. The switch is achieved by the power relay RLB which is on in high power mode. Also via D4 it changes the reference for the operating point of TR10, 11. In low power mode the output via RLB1 through the VSWR/power detector (T4, T5 and associated components) and RLA2 to the r.f. out. In high power mode (RLB energised) the output from T2 goes via RLB2 to T3; after the amplifier output at T6 the output is fed to the r.f. output socket via RLB1, the VSWR/power detector, and RLA2.

9 The VSWR/power detector provides two signals to the central control unit 4 PMF (forward power) and PMR (reverse power).

10 Overtemperature protection is provided by R19, TR8 and TR13. R19 is a thermistor and senses the temperature and TR13 turns the r.f. to low power in the overheat condition.

11 TR5, the Pre-Driver, and TR10, 11, the Driver Power Amplifiers, are operating in Class A bias to minimise harmonic generation. TR18, 19 is a standard power amplifier for high power mode using sliding Class A bias operation to conserve battery life.

IF AMPLIFIER (UNIT 2) See Figs 4, 6.

Introduction

12 The IF unit performs all the necessary conversions to:

(1) In the transmit case, convert the base band signal to the SSB signal required to drive the transmitter power amplifiers.

(2) In the receive case, to take the antenna r.f. signal (SSB) and to provide the conversion and processing to yield the detected base band signal for subsequent processing by the audio board.

13 The system employed in both the transmit and receive cases is double conversion using a 90.023 MHz roofing filter to provide second image rejection and a 1.4 MHz LSB filter as the channel filter. The base band conversion uses four-quadrant multipliers in both the transmit and receive cases.

14 Gain control is provided by varying the local oscillator drives to the first and second mixers. The oscillator drive to each mixer is varied by pin diode attenuators. Each attenuator has its series and shunt arms separately driven with currents obtained from the AGC Driver Assembly Unit 2b.

15 The AGC Driver Assembly is an analogue computer which converts the a.g.c. signal at GCF to the specific currents required for each pin diode system.

Power Supply

16 Battery power is taken from PL7 pin 9 to the series regulator transistor TR19 emitter. The output voltage of TR19 is divided by three using R75 and R76 and compared with the reference voltage using IC12. The control signal from IC12 is fed back via TR20 to the base of TR19.

17 The reference voltages and power for IC12 are obtained from BSW at PL7 pin 8. Thus, when BSW is high, i.e. at battery voltage (24 V nominal), the stabiliser is enabled. Conversely, when BSW is low, the stabiliser is switched OFF. The resulting 20 V stabilised output is fed to the bus at PL7 pin 16 and is also used to power the internal unit 2 systems.

18 The second stabiliser employs TR18 as a current bypass regulator to provide a constant nominal 8 V drop between the collector and the emitter of TR18. The 8 V drop is maintained even if the 20 V regulator saturates, which occurs when the battery voltage falls below 20 V.

19 The output voltage is scaled using the voltage divider R71, R72 and then fed to IC12b for comparison with the reference voltage. The output of IC12b drives the base of TR18. The reference voltage is obtained from the reference diode D15 which is fed from the constant current diode D14.

NOTE:
This output will be referred to as 12 V constant. The internal lines 12VRX, 12VTX are both derived from 12 V constant.

Transmit/Receive Switch

20 The transmit/receive switch is operated from the CPS signal at PL7 pin 7. In the receive condition CPS is low (0 V) and the output from TR4, 12 V Rx, is enabled. The 12 V Rx supply is applied to the mirror system TR5/TR6, which is the reference mirror for the currents for the working r.f. stages. This enables TR2,R3/TR9,R24 and TR13,R32 as constant current sources

21 Similarly in transmit, with CPS high (5 V) the 12 V Tx is enabled and is applied to the mirror system TR7,TR8 which then enables TR10,R25/TR11,R31 and TR14,R37 as constant current sources.

Receiver Signal Processing

22 The received signal RSI enters the board at SK4 via the protection diodes D19-D22, through the low pass filter (30 MHz cut off) L2,C2,C4,C7 and via T2 to the sources of the double balanced first mixer.

23 The LO1 drive is fed to the gates in push pull via the attenuator system which is used for a.g.c. purposes.

24 The output from the mixer drains is tuned by T6 and then fed via 2gD1 to the 90 MHz first IF filter. Variation of the local oscillator drive at the gates varies the conversion gain of the mixer, and hence provides part of the a.g.c. control function.

25 From the output of the 90 MHz filter the IF signal passes via D2 and T7 to the sources of a push pull grounded gate amplifier IC3. The output of IC3 is tuned and matched by the push pull transformer T9 to a similar stage IC5 which is identical except for additional a.g.c. capability provided by pin diodes 2eD1 and 2eD2 in the output circuit T11.

26 Under low signal conditions TR12 conducts all the current required by IC5 and as a consequence no current flows through 2eD1 and 2eD2, which are accordingly in a high resistance condition. When, however, this segment becomes active, TR12 progressively comes out of full conduction and the system current for IC5 is shared between TR12 and 2eD1,D2, which reduces the gain of the IC5 amplifier by damping the output circuit.

27 The bias for TR12 is derived from the analogue computer within the AGC Driver Unit 2b.

28 The output of the amplifier IC5 feeds the sources of the Receiver 2nd Mixer IC7.

29 The LO2 signal drives the gates of IC7 via the transformer T14, a.g.c. is provided, as for the 1st mixer by modulating the level of the LO signal in order to vary the conversion gain of the mixer.

30 When the system is operated in USB mode the LO2 frequency is nominally 88.624 MHz, whereas in LSB mode LO2 is nominally 91.423 MHz.

31 In both instances the wanted signal output from IC7 is 1.4 MHz LSB. The output from the drains of Mixer 2 (IC7) is tuned and matched by T15 and fed via 2dD1 to the sideband filter (1.4 MHz LSB) FL2.

32 The second IF signal at the output of FL2 is fed to IC9 which operates as a grounded gate amplifier stage, the output of which is tuned by T18 (assembly unit 2c). The output of T18 is fed to the signal input port of the receiver demodulator IC11.

33 The 1.4 MHz LO3 signal is taken from port 2PL5 to the IC11 carrier input port. The resulting base band output is fed via the a.f. amplifier IC13a and IC13b to the AFR output.

Transmitter Operation

34 The a.f. signal (AFT) enters the board at PL7 pin 17 and is a.c. coupled to the signal input port of the double balanced modulator IC10. The 1.4 MHz LO3 signal is fed to the IC10 carrier input via PL5. The output which is obtained at T19 is a double side band suppressed carrier signal.

35 This signal is fed to the emitter follower TR15 and thence to the gates of IC9. In order that IC9 shall operate now as a source follower, it is necessary that the tuned load T18, which was employed in the receive condition, be short-circuited. This is done by causing TR16 to turn off. When TR16 is in the off condition all the current required by IC9 now flows through pin diodes D8 and D9, which provide an a.c. short circuit to ground from the drains of IC9. TR16 is turned on and off by using TR17 to level shift and invert the 12VRX command.

36 The output of the source follower IC9 is fed via T17 to the sideband filter 1.4 MHz which removes the unwanted sideband. The resulting lower sideband signal is then passed via D3 to the second transmit mixer. As in receive, a.g.c. is obtained by modulating the LO2 drive level.

37 Upper and lower sideband selection is performed by changing the LO2 frequency to 88.624 MHz nominal or 91.423 MHz as appropriate (as in receive operation).

38 The frequency of LO2 is varied by the synthesizer to obtain the 100 Hz frequency increment.

39 The LO2 mixer output is tuned and matched to the succeeding amplifiers IC6 and IC4, which are push pull grounded gate amplifier stages. The output of IC4 is switched to the roofing filter (90.023 MHz) by 2kD1. The roofing filter attenuates the image frequency of the second mixer. The filtered signal is switched by D1 to the first Tx mixer.

40 The LO1 level is not varied in the Tx mode, all a.g.c. activity is via LO2 control.

41 The resulting signal frequency is passed through a 30 MHz low pass filter L1,C1,C3,C6 to the output TSD at SK3.

Attenuator Systems and AGC Driver Assembly

42 The LO1 and LO2 attenuator systems are similar in form. Each attenuator system consists of a bridged T section and a half section. There are four pin diodes, used as current dependant variable resistors, in each attenuator system. Power is derived from the 20 V line, the current flowing through the diodes being under the control of variable current sinks to the 12 V constant line. There are two sinks for each system, one to control the current in the series arm diodes, and one for the shunt arm diodes.

43 The AGC Driver Unit 2b (see fig. 6) employs two identical analogue computing systems. Each system uses matched transistors (within integrated transistor arrays) as log and antilog elements to perform the necessary operations.

44 A current of approximately 200µA is obtained from the current mirror IC4 and fed to the a.g.c. line (GCF) through R19 and R20 which therefore produces constant offset voltages relative to the voltage at GCF, the control voltage.

45 For section one a constant current is obtained from IC2d collector which then drives a transistor pair IC2a,IC2c so as to produce two currents of constant ratio. As GCF is varied IC2d saturates and the current is no longer constant, but the ratio at the collectors of IC2a and IC2c remains constant.

46 These currents produce in IC6d Q5 and IC7 Q1 voltages proportional to the log. of each current. Since IC6 Q5 and IC7 Q1 are in series, the voltages and hence the logs are added. Since IC6 Q3 and IC7 Q2 are also in series, and the voltages are identical, a current proportional to the product of the currents is produced at the collector of IC7 Q2. This current is used to modulate the current mirror system IC11,IC15 to produce a variable current sink at 2b pin 9.

47 By a similar reasoning, the current at the collector of IC8 Q1 is proportional to the inverse of the current in IC7 Q2. This current modulates IC13/IC17, the variable sink at pin 10. The currents at pins 9 and 10 vary the currents flowing in the shunt and series arms of the attenuator for LO2.

48 The LO1 attenuator system is driven by an identical system, but its threshold is delayed by the amount of the voltage drop across R20. The remaining control element IC2b Q3 becomes active at low values of GCF and via the current mirror IC1 modulates the bias current available at pin 5. This causes 2a TR12 to come out of saturation (see paras 26 and 27).

DC Operation

49 Extensive use of d.c. stacking is employed in this unit to facilitate TR switching.

50 In the receive state, as has been explained, biasing TR2 enables a constant current of about 17mA to the sources of the first Rx mixer - via the centre tap of the input transformer T2. This current is used to power the first RX mixer, IC1, and the first 90 MHz amplifier, IC3.

51 The 12 V Rx supply is used to bias gates 1 and 2 of IC3. IC3 then acts in d.c. terms as a source follower, which then defines the supply voltage of IC1.

52 The current through IC1 and IC3 also flows through pin diodes D2 and 2gD1, which are then in a low resistance condition. As a result the input signal is routed from the first mixer, IC1, to the amplifier, IC3, via the 90 MHz filter.

53 Similarly in Transmit TR10 enables a constant current to the 90 MHz transmitter amplifier IC4 and the final mixer IC2.

54 The 12 V TX supply biasses the gates of IC2 which then acts in dc terms as a source follower providing the supply voltage to IC4.

55 The current now flowing through IC4 and IC2 also flows through D1 and 2kD1. The diodes D1 and 2kD1 are accordingly in a low resistance condition. As a result the transmitter 90 MHz signal is routed to the final TX mixer via the 90 MHz filter.

56 In TX 2gD1 and D2 are reverse biassed by R12 and R13 and consequently are in a high impedance condition. Similarly in RX D1 and 2kD1 are reverse biassed by R11 and R15.

SYNTHESIZER (UNIT 3) See Fig 8

57 The frequency synthesizer has to produce three local oscillator signals which are used by the IF board. Two of these signals, LO1 and LO2, are generated by two phase locked loop frequency synthesizers whilst the third, LO3, is merely a fixed divider from the TCXO.

Frequency range of	LO1	91.523 - 120.022 MHz
	LO2	88.624 - 88.6231 MHz (USB)
		91.423 - 91.4221 MHz (LSB)
	LO3	1.4 MHz.

58 LO1 moves in 1 kHz steps, while LO2 moves in 100 Hz steps for both USB and LSB. LO3 is a fixed frequency.

59 ML1 TCXO provides the reference frequency for the two phase locked loops at 5.6 MHz. The frequency is adjustable, to take out the effects of aging, by R19. The supply to ML1 is provided by a voltage regulator circuit R20, D2, TR10 from the 20 V supply to provide 12.5 V nominally.

60 The output of the TCXO is capacitively coupled and R23, R18 potential divider provide the correct DC voltage to interface with the TTL input levels on IC1, IC5, IC3.

61 ML1 output goes to the clock inputs of IC3 which has two D type flip-flops configured as a Johnston counter to give a divide-by-4. The output from IC3 via attenuator R22 goes to LO3 port, this is terminated by 50 Ω within the IF unit.

62 The two synthesizer chips IC1 and IC5 (BCC024) need to be loaded with data for their counters. The data comes from the central control as a 32 bit serial word, the first 11 bits sent with the frame low.

63 IC6 is configured as a demultiplexer such that while SYF (PL7/14) is low, SYC (PL7/2) is gated through IC6c to clock 2 (IC1 Pin 2, IC5 Pin 2). When SYF is high (5.25 V), SYC is gated through IC6b to clock 1 (IC1 Pin 14, IC5 Pin 14). The falling edge of the frame latches the data into the internal counters.

64 When the synthesizer is in lock the outputs from the BCC024 YZORD, YOZ and YOZ D'LYD will all be low. (YZORD is high, when the synthesizer is out of lock and provides the SYL signal via D1 or D4). The BCC024 provides two output signals to correct the frequency of the oscillator, PUMP UP (Pin 6) and PUMP DOWN (Pin 7).

65 TR6, 7, 8 and 9 plus associated components make up the current pumps. If the PUMP DOWN output is taken low a current will flow out of the loop filter (C8, C6 and R9) the magnitude of the current is defined by the base voltage of TR7 and the resistance R11 plus the On resistance of the output (125 Ω typ).

66 If the PUMP DOWN output is taken low then current will flow through TR9, the magnitude being defined by the base voltage and emitter resistance (R17 plus the output stage on resistance). This current will be passed through the current mirror TR6, TR8 and therefore a current of the same magnitude will flow into the loop filter.

67 The voltage on the loop filter will be modified by these currents. This voltage is applied to the source follower buffer TR1 and then from the buffer to the V_t line of the oscillator 3b.

68 When the synthesizer is out of lock YZORD (Pin 4) output is high which will boost the magnitude of the current pumps by increasing the base voltage of TR7, TR9 as R14 is taken to 5.25 V. TR4 will also be switched in initially until the loop is approaching lock when it will turn off and TR2 will be switched in for a further three comparison cycles. After this TR2 and TR4 will both be switched out whilst the loop stays in lock.

69 3bTR1 with tuned circuit 3bL1, D1, D2 and C1 produce the oscillator circuit. 3bTR2 is in grounded base and is a buffer for the oscillator. The RF current in the collector of 3bTR1 is split by resistors 3aR2 and R8 into two further grounded base buffers TR3 and TR5.

70 The signal at the collector of TR3 passes through a filter made up of C45, L2 and L1 to the LO1 output for the IF unit. The signal at the collector of TR5 passes into IC2 which is a dual modulus prescaler (÷ 40/41).

71 The modulus control is provided by the BCC024 (high out of Pin 12 is ÷ 41) and the output from the prescaler is then connected to the input (Pin 11) of the BCC024 synthesizer chip.

72 The LO2 loop works in a similar manner to the LO1 loop as described.

73 TR11, R21, D3 provide the regulated voltage from the 20 V supply for the current pumps and V_t buffer circuits, nominally 15.5 V.

CENTRAL CONTROL (UNIT 4) See Fig 11

74 The majority of circuits on this board are powered at a voltage of 5.25 V; which is produced by a switched mode power supply, comprising of IC10, T1 and associated components.

75 The input is taken from the BSW supply at a nominal 24 V, and the regulated output voltage can be set by R9 (to 5.25 V). The switching rate is about 25 kHz, with a variable mark/space ratio, dependent on both input voltage and output current.

76 The main circuit on this board consists of a microprocessor IC8 with associated ROM IC1 and RAM IC2. Selection of ROM and RAM is done by the Memory decoder chip IC7 (CDP 1882), controlled by the microprocessor address lines:

IC1 (27C32) ROM (CS0 low) & 0000 - & 0FFF
IC2 (5517) RAM (CS1 low) & 1000 - & 17FF
IC8 (1805) RAM (CS2 low) & 2000 - & 203F
(CS3 is not used)

77 Selection of the input/output peripherals is done by the I/O decoder chip IC9 (CDP 1873), controlled by the microprocessor N lines:

N = 0	Q0 = 0	Not used
N = 1	Q1 = 0	Start A/D converter (No read or write)
N = 2	Q2 = 0	Read A/D converter
N = 3	Q3 = 0	Write to D/A converter (GCF output)
N = 4	Q4 = 0	Write to IC14 latch (CPS and AF volume)
N = 5	Q5 = 0	Write to IC16 latch (TUS and A/D Multiplexer selection)
N = 6	Q6 = 0	Write to IC15 latch (CPL, TNE, MSA, Key)
N = 7	Q7 = 0	Write to IC13 latch (Synth lines).

78 Selection of the input to the A/D converter is done by IC11 (CD 4051) which is controlled by Q3 and Q4 on the IC16 latch, and Q1 on the IC14 latch.

IC14 Q1	IC16 Q3	IC16 Q4	Measurement	
0	0	0	ATU line voltage	)
0	0	1	GCF voltage	) Receive
0	1	0	PMR (Not used)	) state
0	1	1	BSW voltage	)
1	0	0	ATU line voltage	)
1	0	1	PMF voltage	) Transmit
1	1	0	PMR voltage	) state
1	1	1	BSW voltage	)

79 The microprocessor clock is controlled by a ceramic resonator (XL1) at 1MHz, which is then divided by IC12, providing an output (Q1B) at 500 kHz to drive the A/D converter clock. No other outputs are used.

80 Storage of the radio variables is done by the RAM (IC2), and in order to preserve these variables when the radio is switched off, or the radio battery removed, the RAM can be kept alive by the lithium back-up battery B1 (nominally 3.6 V). Diodes D1, D2 switch the source of supply to the RAM, and deselection of the RAM (when the radio is off) is done by IC5c.

81 Control of the synthesizer is done by 5 V logic on four wires (SD1, SD2, SYC, SYF), all produced by latch IC13. These wires are all normally at 0 V when the synthesizer is not being addressed. In order to set up the synthesizer, two 32 bit words are sent simultaneously on SD1, SD2. SYF is low for the first 11 bits, high for the later 21 bits. SYC provides a rising edge in the middle of each data bit, and is used to clock the 32 bits of data into the synthesizer. The data rate is about 2 kB/s.

82 Control of the radio audio volume (AF1-AF3) and internal Transmit/Receive (CPS) is done by IC14 latch, also with 5 V logic.

Minimum volume is given by AF1, AF2, AF3 = 0
Maximum volume is given by AF1, AF2, AF3 = 1
Default volume (level 3) on switch on AF1, AF2 = 1, AF3 = 0.

83 CPS is used internally to control the Transmit/Receive function and is low for Receive, high for Transmit.

84 Control of the radio power level (CPL), Error tone enable (TNE), Mode selection (MSA) and the internal keyline is done by IC15 with 5 V logic.

CPL	0 = Low power selected	1 = High power
TNE	0 = Error tone off	1 = Error tune enabled
MSA	0 = CW selected	1 = Voice selected
Key	0 = Normal operation	1 = Tune requested.

85 TR5 is used to invert the Key which is then OR'd with KCW, allowing the Tune requested information to be exported.

86 Control of the ATU (Via TUS) and the keyboard (via KBS) and internal control of the A/D multiplexer are done by IC16 with 5 V logic.

87 ATU signalling is effected by using TR4 to provide a short circuit on the TUS line (which has an 820 Ω pull-up resistor to +24 V on the AF board). The format of the word to the ATU is a pulse width modulated stream at 250 baud rate (i.e. 1 ms per quarter segment). IC16Q1 is normally low, and is only pulsed high when an ATU tune is required.

88 KBS signalling is also affected using a pulse width modulated data stream. However, in this case the rate is at 1 kB/s (i.e. 250 µs for each quarter segment of the bit being sent). During periods of inactivity, KBS is low (0 V). If a message is to be sent by the central control to the keyboard, TR1 is enabled by IC16Q2 and IC8Q is used to send the data out; after which TR1 will be disabled again. However, if a message is to be received on KBS by the central control, it will be passed via IC5b to the microprocessor EF1 input for decoding. IC5b is used to select either KBS or KVO for decoding according to the state of Q.

IC16Q2 = 0	Q = 0	KBS to be decoded
IC16Q2 = 0	Q = 1	KVO to be decoded
IC16Q2 = 1	Q = Data	KBS being generated.

89 D6, D7 are used to prevent KBS exceeding the permissible voltage limits, and R20 (47k) provides a pull down resistor to ensure that the line is low when inactive. For a fuller discussion on the protocol and signalling on this line, refer to Appendix 1 of this chapter. IC16Q3 and Q4 have been referred to in Paras 77, 78 and are used to select the A/D multiplexer.

90 In the receive state, the voltage on GCF is monitored (at intervals of about 50 ms) by the A/D converter, causing the microprocessor system to output a KBS signal containing bar display information, which is an assessment of Receive signal strength.

91 The KCW line is also monitored (via the processor INT pin) to determine if a change to Transmit is requested via the pressel. Should this happen, the Interrupt service routine is entered, and the necessary outputs are changed to cause the radio to transmit. (CPS high, new synthesizer words if appropriate, minimum AF volume and minimum GCF during the transition).

92 During Transmit, the forward and reverse RF power levels are detected on the PA board, and the resultant analogue signals are passed via the interconnect to the A/D converter. Calculation of the correct level for GCF output is done by the microprocessor system based on the PMF, PMR and BSW measurements, giving an output RF power level dependent on both VSWR and battery voltage. The PMF and PMR sensor levels are modified by TR2 and TR3 when high power is selected, effectively attenuating the levels to values within the A/D converter range.

93 The KCW line is also monitored (via the processor INT pin) to determine if a change to Receive is needed by release of the pressel. Should this happen, the necessary outputs are changed to cause the radio to receive (CPS low, GCF to maximum, minimum AF volume during the transition.

94 The microprocessor also monitors the out-of-lock line from the synthesizer (SYL), which is multiplexed with the keyboard frame pulse (KFR) by IC5a. If the synthesizer is out-of-lock (SYL=1), then transmission is inhibited, and the Error tone enabled.

95 The front panel switches are also monitored by the microprocessor via the two control lines SWA and SWB, with pull up resistors R24, R27 (47k). For a table of voltages for these pins, refer to Audio (Unit 5A) paragraph 99.

96 The D/A converter (IC4) is only used actively during transmit. Because the outputs on Pins 11 and 12 are current sources, an operational amplifier (IC6b) is used to convert these differential currents to a voltage output, varying between 2.5 and 5.25 volts. During receive, the output level is set to maximum and control of GCF is done by the AF board, with D3 being back biassed, isolating the D/A from control.

AUDIO (UNIT 5A) See Fig 13

Introduction and Control

97 The audio board contains all the low frequency processing of the BCC 39 series radio. The system is controlled primarily by the system switch, which has five positions: Z, Off, Aux, 1F, 2F. This switch also enables power supplies on the a.f. board for local use, using BSW, which also enables the rest of the radio. Also enabled is the auxiliary output at pin C of the a.f. socket.

98 The state of the system switch is signalled to the central control system using SK6 lines SWA and SWB (excluding the off position, since the microprocessor is not active in this condition).

99 These commands together with the keyboard and pressel information states are processed by the central control, which then sets the required condition of the audio board using 5 V logic signals on the interconnect system.

Signal Switching System

TABLE 1

Signal Switching

	SWA	SWB	BSW	C
ZERO	1	1	BATT	0
OFF	-	-	0	0
AUX	0	1	0	BATT
1F	1	0	BATT	BATT
2F	0	0	BATT	BATT

100 The supply at pin C of SK1/2 has an overcurrent trip to provide protection. When AUX, 1F or 2F is selected, forward bias is applied to the gate of TR1 via the resistive divider R13/R14. If the current through TR1 is low, the voltage returned to the base of TR22 through R10 is insufficient to turn TR2 on. When, however, due to excess current, the voltage drop across TR1 becomes sufficient to turn TR2 on, TR1 is then turned off. The voltage at pin C then falls to a low value and TR2 is then latched on.

101 A separate circuit is necessary with this system to reset or set TR1 to conduct. This is provided by TR3,C35 and the divider R23,R24. On initial switch-on TR3 is turned on for a short period to temporarily disable the overcurrent protection by preventing TR2 from conducting. TR3 remains on until C35 is fully charged.

102 BSW is turned on via the system switch, which by grounding DU4 causes TR6 gate to be forward biassed and TR6 to turn on.

103 BSW, when enabled, powers the internal 15 V and 7.5 V series stabilisers, TR9 and TR13, with associated components, respectively. Both use operational amplifiers in the feedback path, IC4b and IC4a respectively, for improved regulation. A common voltage reference diode D3 is used for both systems.

Mode Switching

104 The primary states of the a.f. board are Transmit/Receive, which is set by CPS, and Voice/CW, which is set by MSA. The control element operated upon by CPS and MSA is IC1.

TABLE 2

Mode Switching

Mode	Input Condition			IC1d Input		Switch States		IC1a-c
	SK1/2F	CPS	MSA	SA/SC	SB	IC1a	IC1b	IC1c
Tx CW	0	1	0	0	0	Y0-Z	Y0-Z	Y0-Z
Tx Voice	0	1	1	0	1	Y1-Z	Y0-Z	Y0-Z
Rx CW	1	0	0	1	0	Y0-Z	Y1-Z	Y1-Z
Rx Voice	1	0	1	1	1	Y1-Z	Y1-Z	Y1-Z

105 Keying the pressel (SK1/2 pin F = 0) causes the central control to enter the transmit state via KCW and export this as CPS = 1. This state will then be held for a fixed period after the release of the pressel.

Transmit CW

106 If CW is selected and CPS = 1, the diode (OR) DU14 cannot affect the state of TR8 because SB and SA/C of IC1d are both low. The state of TR8 then depends entirely on the state of SK1,2 pin F/KCW. When pin F is low, TR8 is off and the CW oscillator IC5 runs and conversely when pin F is high TR8 is on and the oscillator is inhibited.

107 The output of the CW oscillator is clipped by DU7 and the output passed to the CW filter IC9c,b,a,d. The filtered output is then routed to AFT via IC1a, amplifier IC8a, IC1c and transmission gate TR27 (see Table 2). TR27 is normally closed and its state is governed by the state of SD1. SD1 is normally low except during data transfer to the synthesizer from the Central Control or during Middle of Message signals which are obtained in radios with adaptive capability (i.e. when fitted to BCC 39C).

NOTE:
Transmit CW is entered when tune is requested from the keyboard. The central control then grounds KCW and sets CPS to 1 (= Tx) for the duration of the tune period.

Transmit Voice

108 Microphone signals enter the board on SK1/2 pin A and pass through r.f. and low frequency filters to the VOGAD (Voice Operated Gain Adjusting Device) circuit IC3. This device holds the peak-to-peak output at pin 8 of IC3 substantially constant for a wide range of signal input levels at SK1/2 pin A.

109 The input threshold level of the VOGAD circuit is modified by IC6 which is controlled by the volume control lines AF1, AF2 and AF3, such that when the volume control is set to maximum the microphone sensitivity is at a minimum and vice versa. The output at IC3 pin 8 is compressed by the circuit IC7d,DU9 and passed to the voice filter IC7a,b,c via the switch IC1b. The output of the voice filter is then routed to AFT via IC1b, amplifier IC8a,IC1c and TR27 (see also Tx CW state).

Transmit Sidetone

110 Sidetone output is taken from IC8a pin 1 to amplifier IC8b via transmission gate TR14, which in transmit mode is under the control of SYF. The error tone as appropriate is summed with the signal at the virtual earth point of IC8b.

111 The output of IC8b passes to the variable attenuator system IC10, which is controlled by the volume control lines AF1, AF2 and AF3. The attenuated output is then split into two paths to drive two independent buffer amplifiers IC8d and c. These outputs are fed via SK1/2 pins D and G to the headphones.

Receive CW and Voice

112 The received signal from the IF system is fed to the AF board via AFR. In receive switch IC1b connects pin 3 and 4, thus the AFR signal feeds the CW filter section and the voice section filter in parallel. Both outputs are then present at IC1a input. Selection between Voice and CW takes place at IC1a under control of MSA (see Table 2).

113 The selected output is then present at TP4 and then amplified by IC8a. Switch IC1c routes the output of IC8 to the AGC circuitry, which then controls the IF system gain so as to maintain the level at IC8a pin 1 constant.

114 The output from IC8a pin 1 to the headphones is identical to that explained in Tx Sidetone.

Error Tone

115 The Error Tone Oscillator IC11 consists of an oscillator section and a divider section. The frequency of the oscillator is modified by switching C95 using TR28 which is switched by the divided oscillator output. IC11 is enabled by control line TNE=1. If TNE is held high, the tone oscillator output is a pair of alternating tones. If TNE is pulsed, the output will be either a pulsed single tone (pips) or a pulsed pair of tones, depending on the period of TNE high.

AGC Receive

116 The signal from IC8a pin 1 is amplified by IC2a and detected using the diode doubler DU5. The detected output is buffered by the voltage follower IC2d (TP2).

117 Under zero signal conditions the output at TR2 is low, thus the output of IC2c is at a maximum. The maximum possible output of IC2 is limited to one band gap above 5VC by DU10(a). The a.g.c. control line GCF maximum is therefore two band gaps above 5VC (DU10a and b).

118 At the onset of a large amplitude input signal the voltage at TP2 initially rises rapidly to much greater than 5 V (the reference voltage of the active loop filter IC2c). DU8 then conducts and the resulting current into the virtual earth at pin 9 causes the voltage at GCF to fall.

119 The fall in GCF voltage reduces the gain of the IF system unit 2, thus reducing the detected voltage at TP2 and hence the forward voltage across DU8.

120 Attack Time Constant During the initial overshoot at TP2, C62 is charged through DU12 and R95. When the a.g.c. system has reduced the voltage at TP2 to near 5 V, TR15 will therefore be off and TR12 will be biassed on. As the value of voltage at TP2 becomes slightly lower than 5 V, the fast attack circuit R57 DU8 becomes inactive (DU8 reverse biassed) and a.g.c. control devolves to the slow circuit (slow time constant) of R56,TR12.

121 Hold On pauses in speech the voltage at TP2 will fall to near zero and TR15 will draw base current from C62 and turn on. The collector voltage of TR15 will then be low and TR12 will therefore be turned off. The value of GCF will not therefore change during short pauses in speech due to this action, until the current from C62 is no longer sufficient to turn TR15 on.

122 Slow Recovery A pause continuing past this point will allow TR12 to be turned on and the resulting leak of current through TR12,R56 out of the virtual earth point IC2c pin 9 will cause the value of GCF voltage to rise and consequently the IF gain to increase until either active control is restored or GCF attains the maximum voltage.

123 Fast Recovery During periods of impulsive interference, such as lightning or ignition effects, high voltage spikes/pulses will be present on the voltage envelope at TP2. If IC2b were not present, the peaks would cause AGC action to reduce the peak values to 5 V. However high peak to mean signals cause IC2b to change state on the peaks. The recovery after the impulse is fast because the IC2b pin 7 rising edge via C46, TR7, TR10 causes TR11 to conduct. This condition persists until C46 is fully charged, at which point TR11 turns off and the AGC reverts to slow mode.

124 The fast recovery circuit is also used in transmit, since the receive a.g.c. state must be cleared on entry to the transmit mode. If this is not performed properly, the transmit power would be affected. Accordingly CPS=1 turns TR11 on and, since the voltage at TP2 falls rapidly, the charge in C52 decays rapidly through TR11 and R57 and the voltage at pin 8 of IC2c rises to its maximum value. CPS=1 applied to the gate of TR17 turns it on and clears the charge in C62 to reset the hold time to the waiting state. Fast decay is similarly caused by SD1 being set to 1.

5 V Constant

125 This is used internally as the reference voltage for the a.g.c. system and is used to power the keyboard via the three-way interconnect SK4 pin 2.

KBS

126 This provides the data highway between the central control and the keyboard at SK4 pins 3 and 5.

30 MHz Low Pass Filter

127 The r.f. input from the power amplifier system is at PL1 and the output at SK3. When BSW is high (radio on) R6 connects d.c. power to SK3 for external services and signalling to external antenna tuning units.

CONTROL (UNIT 7) See Fig 15

128 This comprises two boards, the Display/Keyboard and the Microprocessor board. The unit can be connected remotely using an extension cable. This has three connections, 5 V supply, two-way data and earth via PL4. The data in is fed to the microprocessor IC3 on pin 24 and data out from pin 4 via TR2 onto the KBS line.

129 The keyboard operates from a 5 V power supply which is supplied from the radio via PL4 Pin 2.

130 The unit consists of a microprocessor 7BbIC3 (CDP1805A) with 64 bytes of internal RAM, an EPROM (27C32) which contains the program for the microprocessor, a keyboard for data entry purposes scanned by the keyboard encoder 7BbIC2 (MM74C923) and a Liquid Crystal Display driven by the display driver 7BaIC1 (PCF 2111T). The display is backlit for operation in low light levels by two light emitting diodes 7Ba D1, D2 (HLMP - 7000).

Memory Map

131 The address bus from the microprocessor 7BbIC3 is decoded using 7BbIC4 (CDP1882) and provides the following memory map:

7BbIC5 ROM (27C32)	$\overline{CS0}$ active	&0000 - &0FFF
(Link LK2 is fitted in the E-F position).		
7BbIC2 KEYBOARD ENCODER	$\overline{CS1}$ active	&1000
7BbIC3 RAM (1805A)	$\overline{CS2}$ active	&2000 - &203F
(Link LK1 is fitted in the B-C position).		
7BbIC1 OUTPUT PORT	$\overline{CS3}$ active	&3000

132 The 18 key switches are configured in a 5 x 4 matrix which is continuously scanned by the keyboard encoder (7BbIC2). If a key is pressed the keyboard encoder recognises the key and puts the 7BbIC2 Pin 13 high which is inverted by 7BbTR1 and causes 7BbIC3 Pin 36 to go low, which causes the microprocessor to be interrupted. The microprocessor may then read from location &1000 to get a code number associated with the key pressed. Fig 2.1 shows the appropriate code number associated with each key. When the key is released the keyboard encoder will remove the interrupt by putting 7BbIC2 Pin 13 to a low level.

133 The LCD is a 62 segment display with two backplanes i.e. 31 bits on each backplane.

134 The display driver is loaded from the microprocessor by two 33 bit words sent sequentially as clock, frame and data. The frame line 7BaIC1 Pin 40 is taken high by 7BbIC1 Q2 before data is loaded.

135 The first 33 bits of data are then sent with a leading zero to 7BaIC1 Pin 39 from 7BbIC1 Q4, and the clock (7BbIC1 Q3) is raised midway between each data bit. The 33rd and last bit specifies the destination of the data word BP1 or BP2, and the frame is then set low and a final clock pulse generated to load the data.

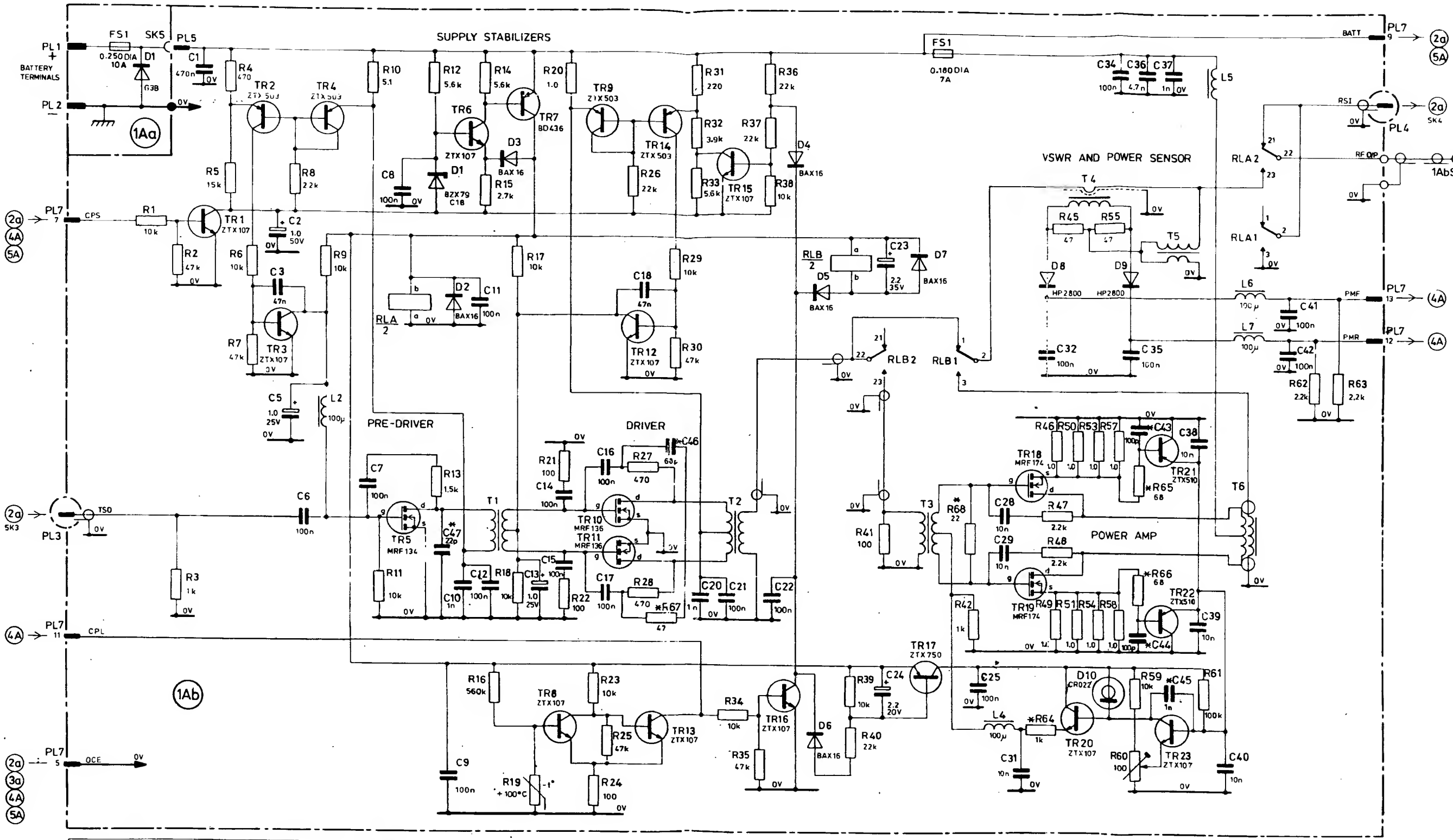
136 The backlighting is controlled by the level on the data line when not sending data to the display driver. If backlighting is required then 7BbIC1 Q4 is left high when not sending data which turns on 7BaTR1 and current flows through 7BaD1 and D2 in series. The current is limited by 7BaR2 to approximately 8 mA. Conversely if the backlighting is not required Q4 is left low when not sending data which will leave 7BaTR1 turned off.

137 Communication between the keyboard and the central control is by way of KBS, a bi-directional serial interface which uses a pulse width modulation signalling scheme with a 1 kbit/sec data rate. The specific format and protocols used are given in Appendix 1.

138 When the keyboard is in the normal listening mode 7BbTR2 is disabled, by 7BbIC1 Q1 being low, and the data is read by the microprocessor on event flag $\overline{EF1}$ 7BbIC3 Pin 24. If the keyboard wishes to send data to the central control then 7BbTR2 is enabled by 7BbIC1 Q1 being high and the pulse width modulation generated by 7BbIC3 Pin 4 Q.

Fig. 2.1 BCC 39 KEYBOARD CODES

UP VOL (05)	CW (09)	0 (01)	1 (11)	2 (0D)	3 (0C)
DN VOL (06)	PWR (0A)	CH (02)	4 (12)	5 (0E)	6 (10)
T (07)	TUN (0B)	SET (03)	7 (13)	8 (0F)	9 (00)



1Aa OR 1Ab THESE NUMBERS PREFIX ALL COMPONENT REFERENCES IN ANY OVERALL DIAGRAM OR TEXT

VIEW FROM BOTTOM

D10

TR 1,2,3,4,6,8,9,12,13,14, 15,16,17,20,21,22 & 23

TR7

VIEW FROM TOP

TR 5, 10, 11, 18 & 19

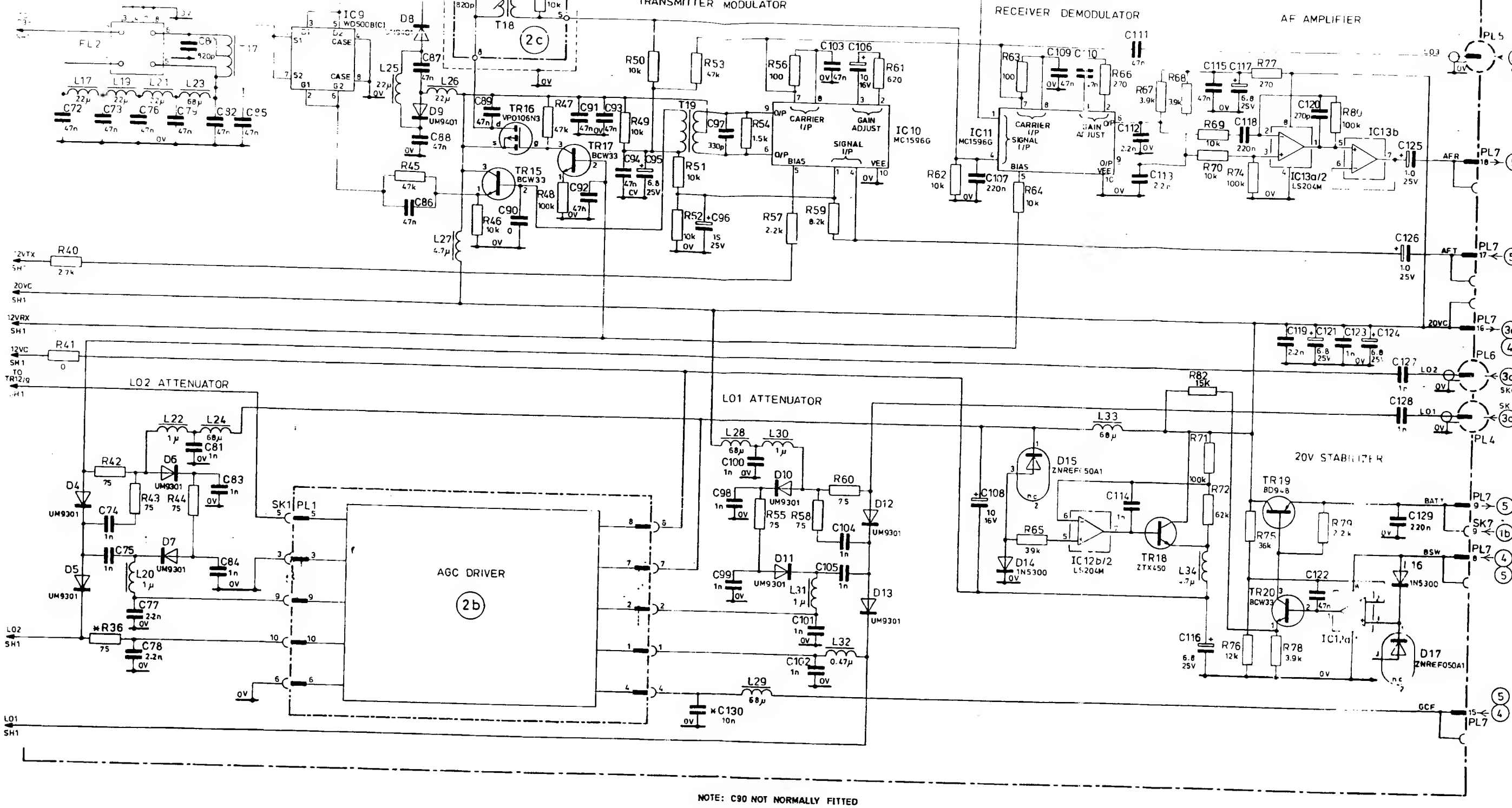
RACAL

TM 9346 | 79270-111-10 | F

BCC 30A

Circuit Diagram: Power Amplifier Unit 1A

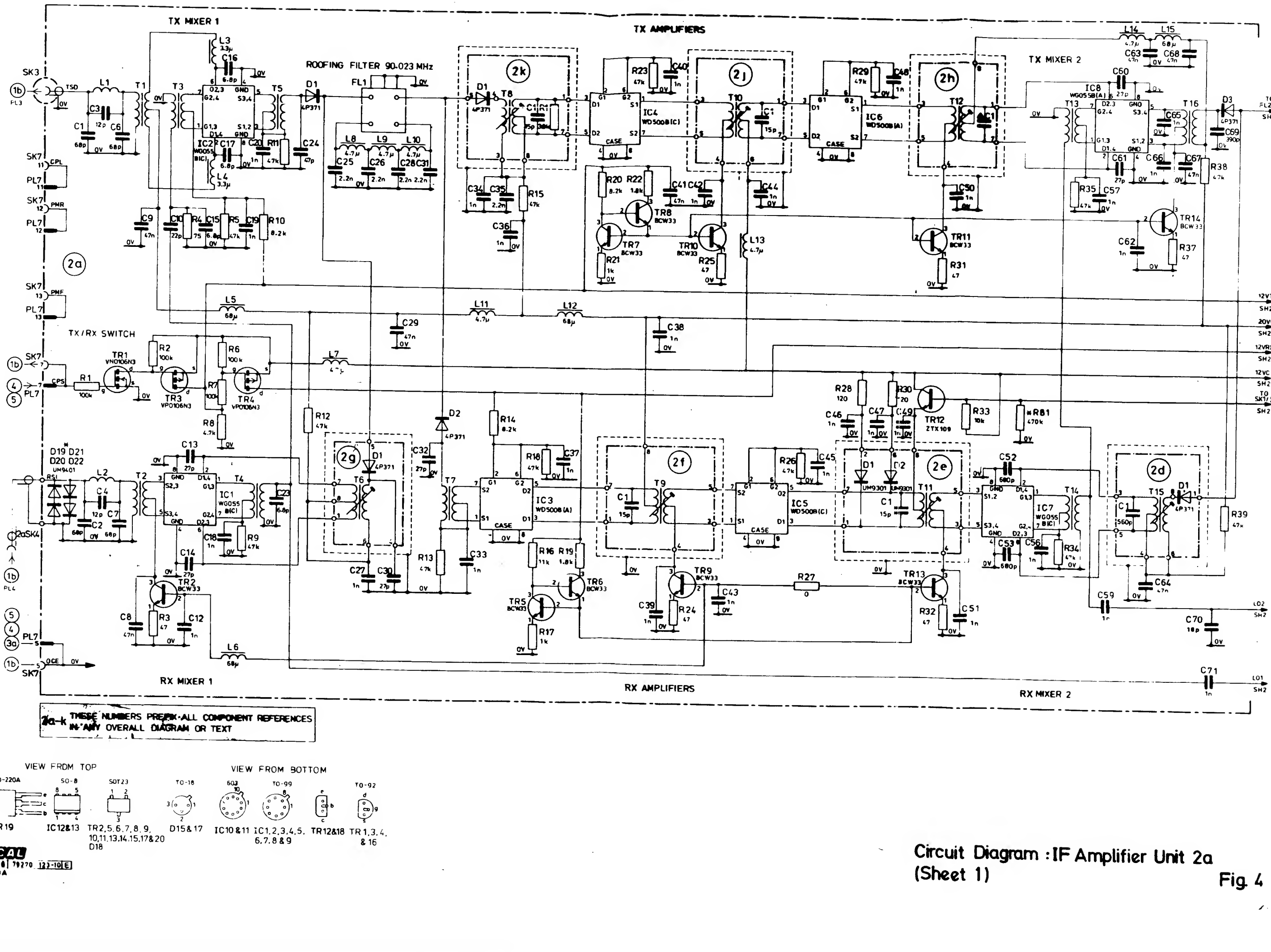
Fig. 1

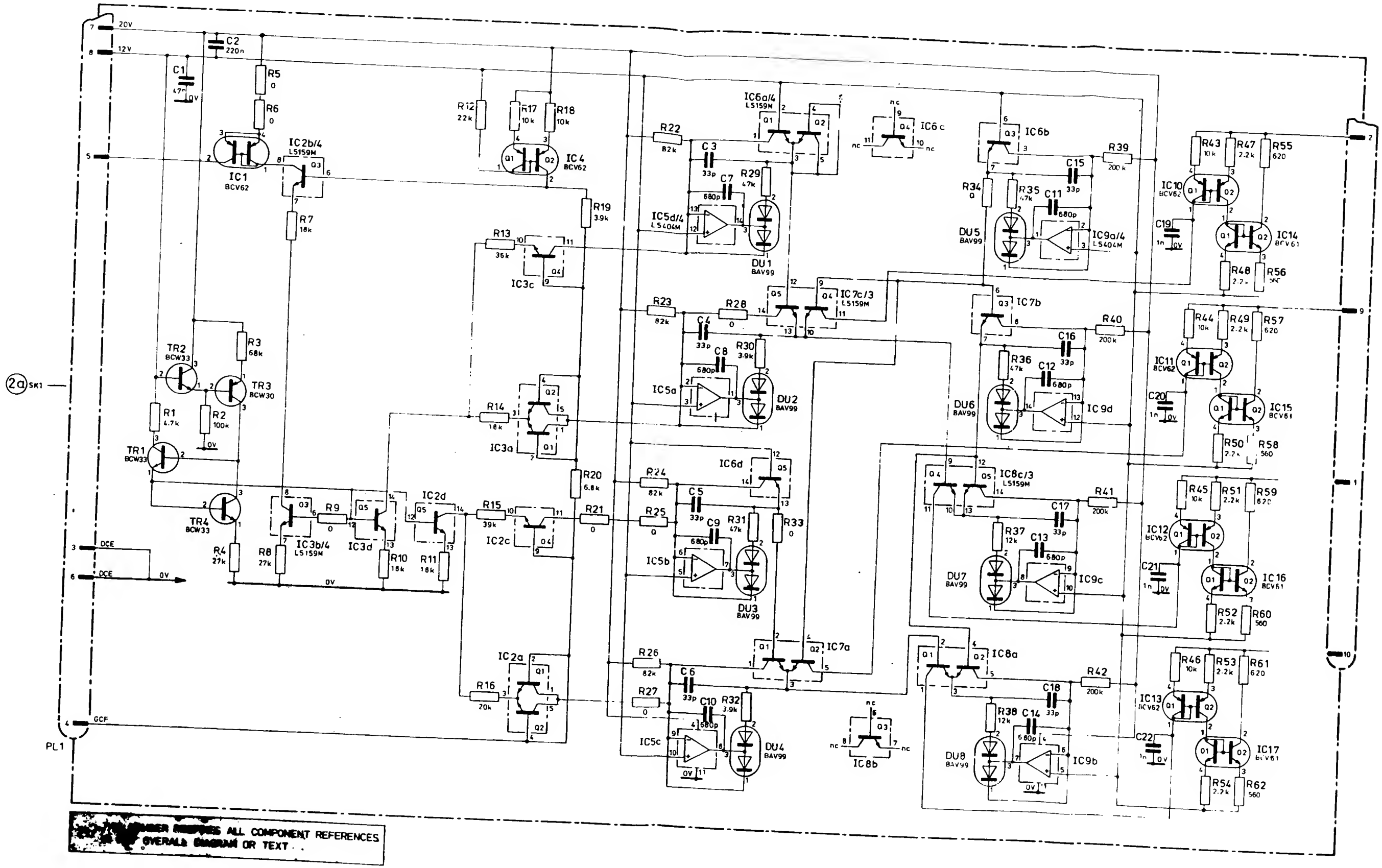


RACAL
TH9346 | 79270-123-10 | E
BCC 39A

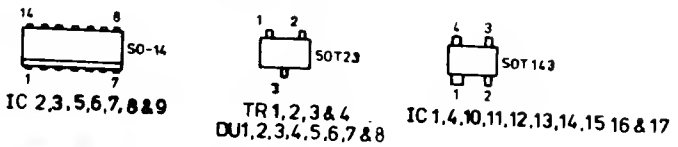
Circuit Diagram : IF Amplifier Unit 2a
(Sheet 2)

Fig. 4


TX MIXER 1
TX AMPLIFIERS
TX MIXER 2
ROOFING FILTER 90-023 MHz
TX/RX SWITCH
RX MIXER 1
RX AMPLIFIERS
RX MIXER 2
2a-k THESE NUMBERS PREFIX ALL COMPONENT REFERENCES IN ANY OVERALL DIAGRAM OR TEXT
VIEW FROM TOP
VIEW FROM BOTTOM
TO-220A
SO-8
SOT23
TO-18
60J
TO-99
TO-92
TR19
IC12&13
TR2,5,6,7,8,9, 10,11,13,14,15,17&20 D18
D15&17
IC10&11
IC1,2,3,4,5, 6,7,8&9
TR12&18
TR1,3,4, &16
RACAL
TH8346 79270 123-10E
Circuit Diagram : IF Amplifier Unit 2a (Sheet 1)
Fig. 4



VIEW FROM TOP

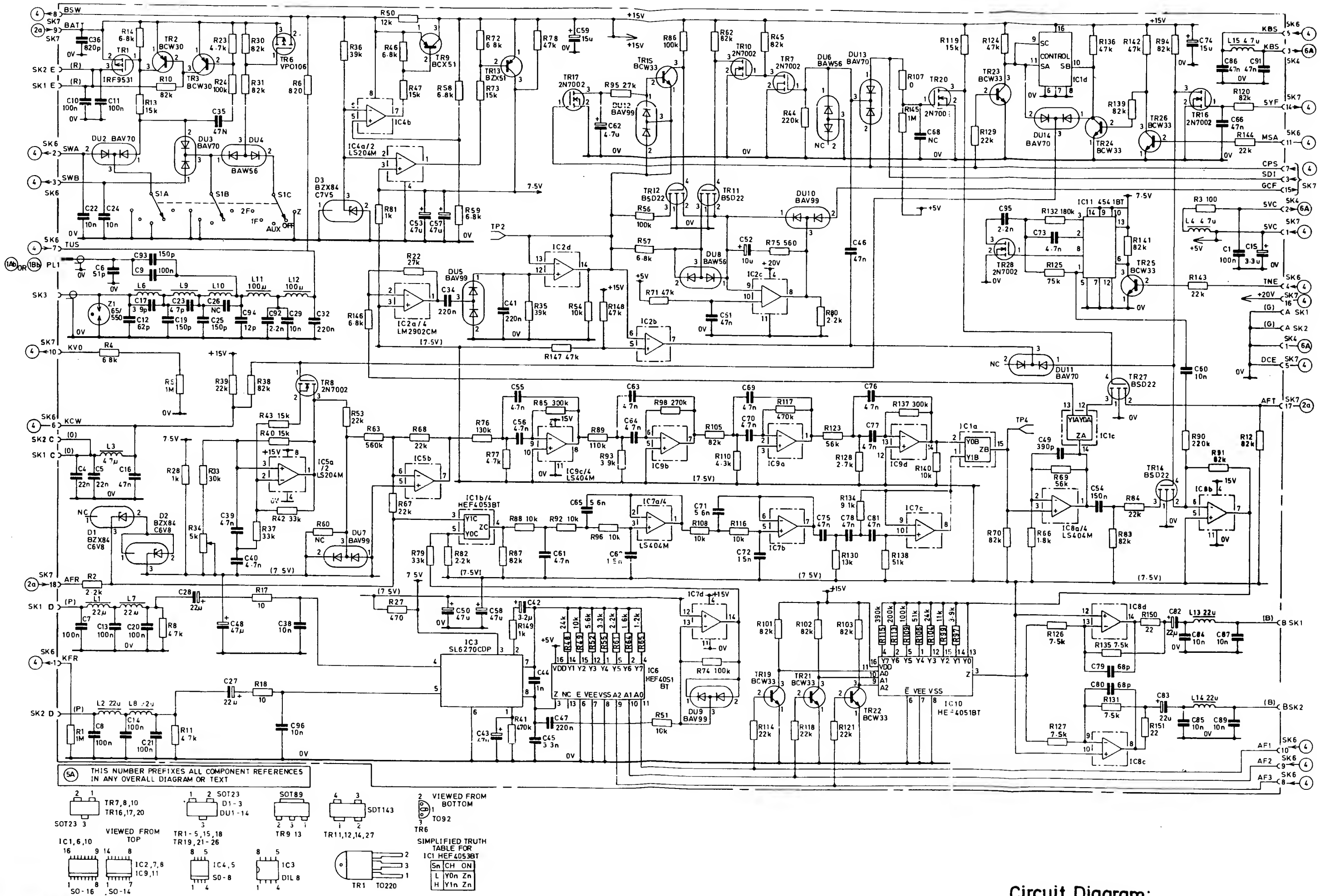


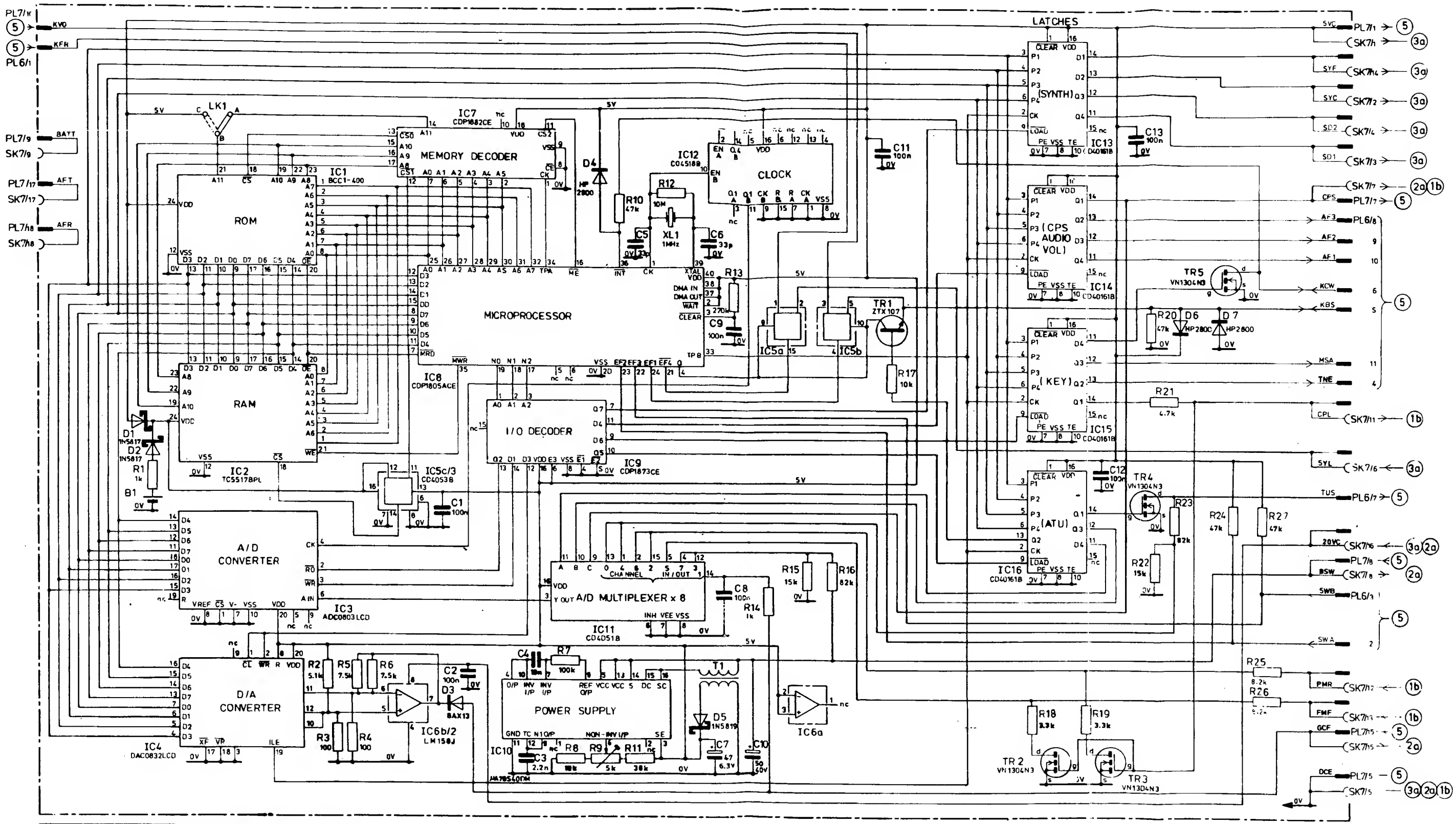
IC 2,3,5,6,7,8&9

TR 1,2,3&4
DU1,2,3,4,5,6,7&8

IC 1,4,10,11,12,13,14,15 16&17

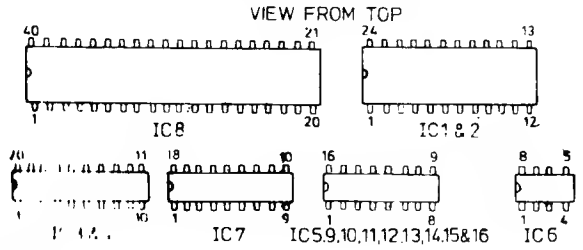
Circuit Diagram : AGC Driver Unit 2b Fig.6


THIS NUMBER PREFIXES ALL COMPONENT REFERENCES IN ANY OVERALL DIAGRAM OR TEXT
TR7,8,10 TR16,17,20
SOT23 3
VIEWED FROM TOP
IC1,6,10
SO-16
IC2,7,8 IC9,11
SO-14
TR1-5,15,18 TR19,21-26
SOT23
D1-3 DU1-14
IC4,5
SO-8
IC3
DIL 8
SOT89
TR9 13
SOT143
TR11,12,14,27
VIEWED FROM BOTTOM
TO92
TR6
TR1 TO220
SIMPLIFIED TRUTH TABLE FOR IC1 HEF4053BT
Sn CH ON
L Y0n Zn
H Y1n Zn
RACAL
TH9346 79270-151-10 J
BCC 39A
Circuit Diagram:
Audio Unit 5A
Fig. 13

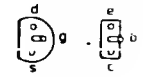


4 THIS NUMBER PREFIXES ALL COMPONENT REFERENCES IN ANY OVERALL DIAGRAM OR TEXT

VIEW FROM TOP



VIEW FROM BOTTOM

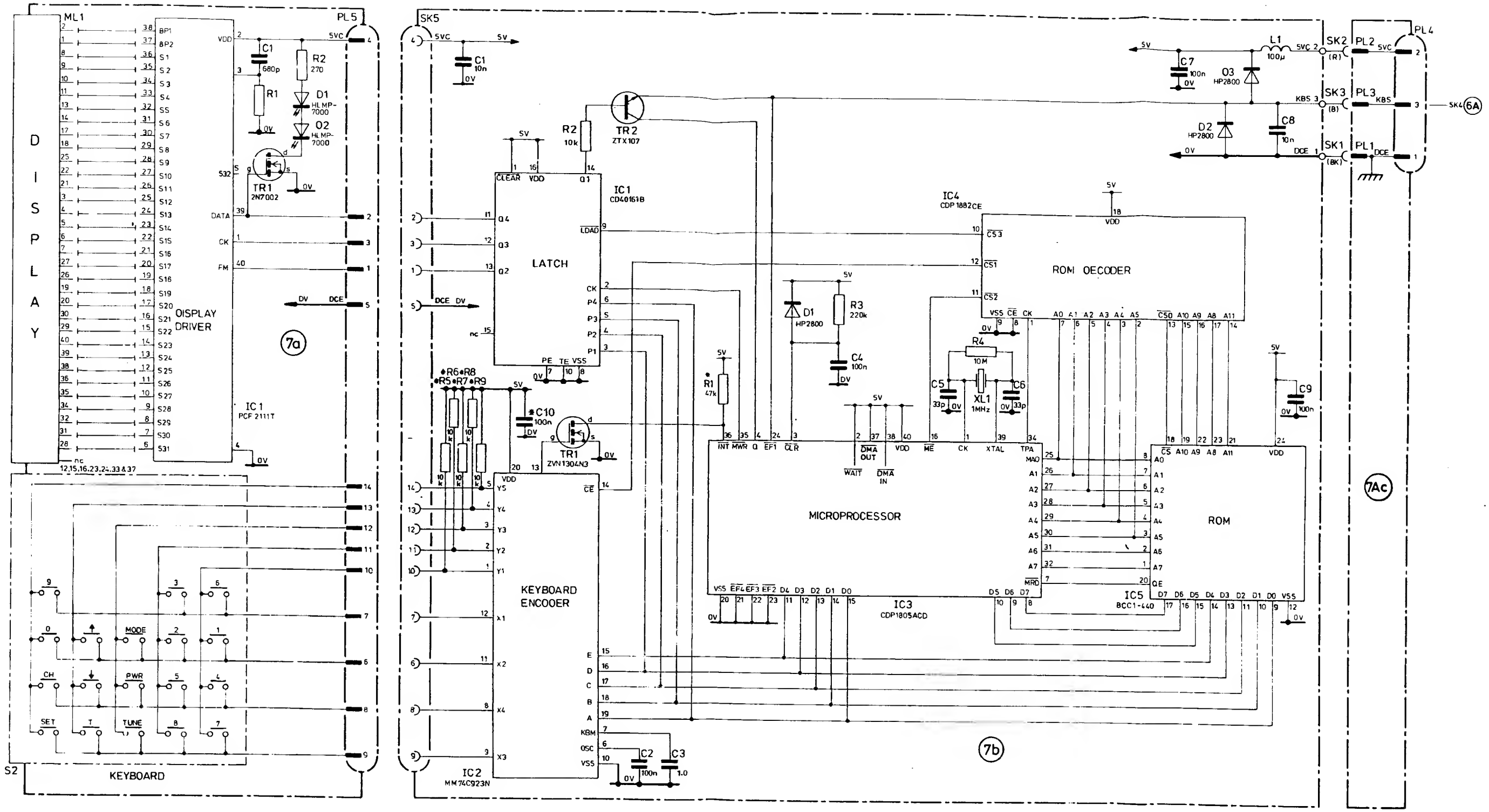


TR2,3, TR1 4&5

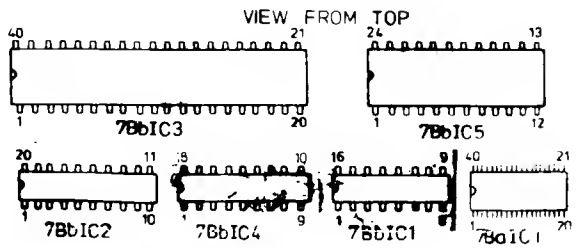
RACAL

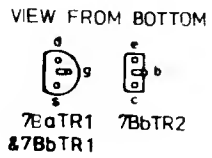
Circuit Diagram : Central Control Unit 4

Fig. 11



7Ba,7BbTHESE NUMBERS PREFIX ALL COMPONENT REFERENCES OR7Ac IN ANY OVERALL DIAGRAM OR TEXT

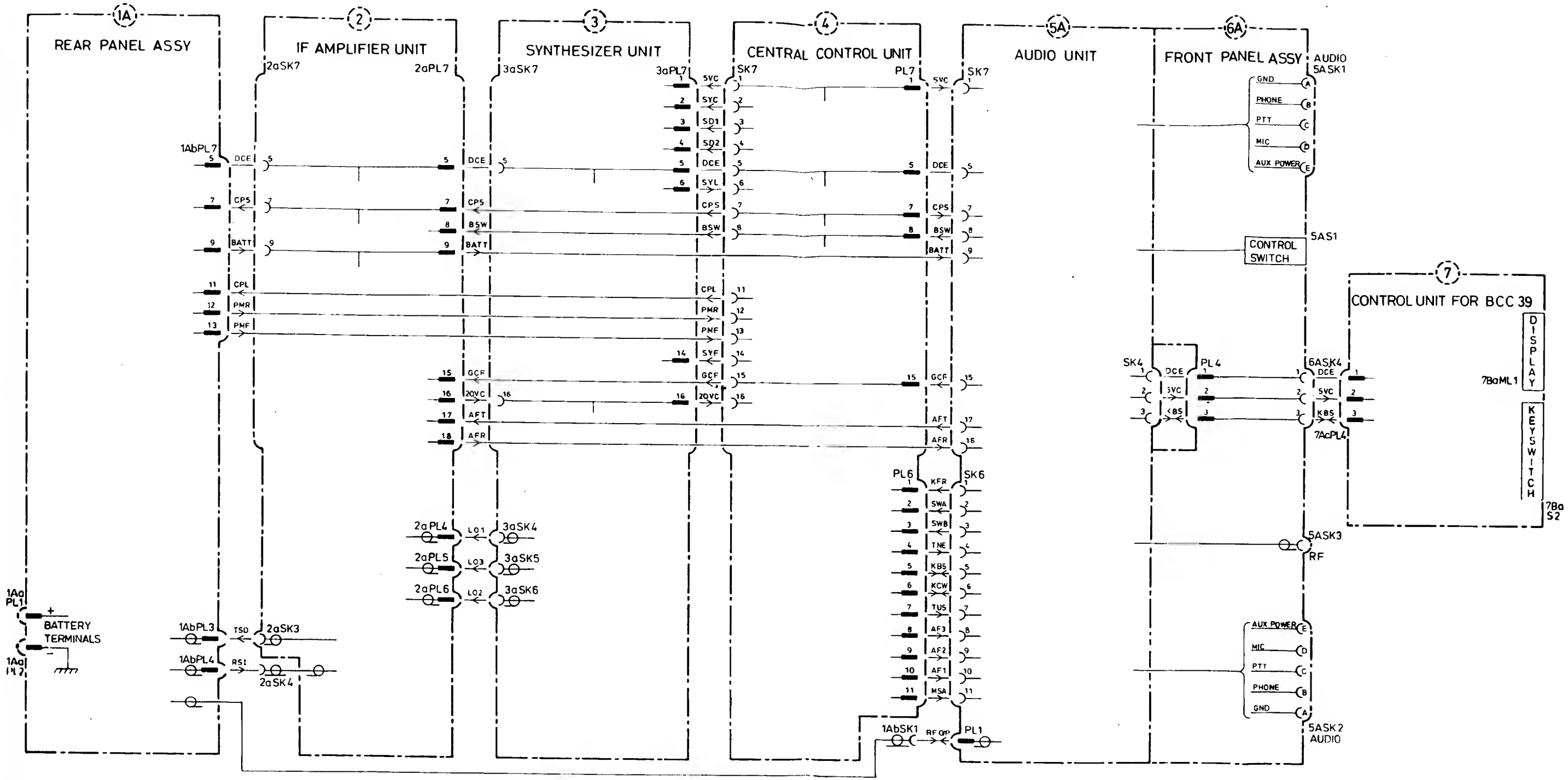




NOTES:-1 FOR BLOCK DIAGRAM SEE FIG 18
2.*DENOTES-REFERENCE NOT IN SEQUENTIAL ORDER.
3.LETTERS MARKED IN PARENTHESES, DENOTE COLOUR OF EQUIPMENT WIRES

RACAL
TH9346 79270-171-09 F
BCC 39A

Circuit Diagram :Control Unit 7 Fig.15



NOTES:-1. 3 OR 4 LETTER CODE - CPL, PMR, BATT etc - DENOTE SIGNAL LINE.
2. THIS BLOCK DIAGRAM TO BE READ IN CONJUNCTION WITH FIG. 4.1

RACAL
1119349 | 78270-102-10 | A
BCC 39A

Interconnection Diagram BCC 39A

Fig. 18

LO1 BUFFERS

LO1 LOOP

1-PRESCALER-2

LO2 BUFFERS

LO2 LOOP

3a,3b THESE NUMBERS PREFIX ALL COMPONENT REFERENCES IN
OR 3c IN ANY OVERALL DIAGRAM OR TEXT

NOTES:- 1. FOR BLOCK DIAGRAM SEE FIG.18
2. * DENOTES. REFERENCE NOT IN SEQUENTIAL ORDER.

VIEW FROM TOP

3aIC1&5 3aIC3&6 3aIC2&4 3aTR6.8 13 & 15

VIEW FROM BOTTOM

3aTR2,4, 18 & 21 | 3bTR1 3cTR1 | 3aTR1,20 | 3aTR3,5, 7,9,14,16, 17 & 19 3bTR2 3cTR2 | 3aTR10 & 11

RACAL
IM9346 79270-131-10 H
ACC 39A

Circuit Diagram : Synthesizer Unit 3